**AMENDMENTS TO THE CLAIMS**:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A microcomputer comprising an internal memory, a central processing unit, and a functional block comprising a peripheral block, built-in said microcomputer, wherein said internal memory has a first program memory and a reprogrammable nonvolatile memory including a first area storing program codes and a second area storing user data, and in which a lock code is written in a specified area; and

the microcomputer has a first mode, wherein the central processing unit fetches instructions from an external memory, and a second mode, wherein the central processing unit fetches instructions from the internal memory and inhibits fetching instructions from the external memory, and comprising:

a first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code;

a logic circuit that performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit; and

a second decoding circuit that decodes the processing mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block, wherein

when a ~~predetermined~~ first value is set into said specified area as the lock code, the microcomputer is configured to be set into the second mode, and

when a second value is set into said specified area as the lock code, the central processing unit fetches instructions from the first area of the reprogrammable nonvolatile memory instead of the first program memory by the reprogrammable nonvolatile memory allocating on the address area to be allocated to the first program memory.

2. (Original) The microcomputer of claim 1, wherein said logic circuit consists of an AND circuit.

3 - 7. (Canceled)

8. (Original) The microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory.

9. (Original) The microcomputer of claim 1, wherein the logic circuit masks the input mode bit by the decoded lock code.